Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1 - 46. (Cancelled)

47. (Withdrawn) A method of forming a two layer LTO backside seal on a wafer having a first side and a second side, the method comprising:

forming a low stress LTO layer on the first side of the wafer; and

forming a high stress LTO layer disposed over the low stress LTO layer.

48. (Withdrawn) The method of claim 47 wherein the step of forming the low stress LTO layer comprises generating a plasma with high frequency RF power and the step of forming the high stress LTO layer comprises generating a plasma with high frequency RF power.

49. (Withdrawn) The method of claim 48 wherein the high frequency RF power in the steps of forming the high and low stress LTO layer has a power between 200 and 1600 watts.

50. (Withdrawn) The method of claim 48 wherein the frequency used in the steps of forming the high and low stress LTO layers is about 13.56MHz.

51. (Withdrawn) The method of claim 47 wherein the pressure used to form the low stress LTO layer is between 200 and 467 Pa.

52. (Withdrawn) The method of claim 47 wherein the step of forming the low stress LTO layer comprises flowing silane into a reaction chamber with a flow rate between 50 and 1000 sccm.

53. (Withdrawn) The method of claim 52 wherein the low stress LTO layer is formed at a temperature between 250 and 600°C.

54. (Withdrawn) The method of claim 52 wherein N_2 is flowed into the reaction chamber with flow rate between 800 and 7000 sccm and N_2O is flowed into the reaction chamber with a N_2O flow rate between 2000 and 18000 sccm.

55. (Withdrawn) The method of claim 47 wherein the step of forming the high stress LTO layer comprises generating a plasma with low frequency RF power between about 0 and 800 watts.

56. (Withdrawn) The method of claim 55 wherein the low frequency used in forming the high stress LTO layer is between 100 and 600 kHz.

57. (Withdrawn) The method of claim 47 wherein the step of forming the high stress LTO layer uses a higher pressure than the pressure used to form the low stress LTO layer.

58. (Withdrawn) The method of claim 47 wherein the pressure used to form the high stress LTO layer is between 200 and 467 Pa.

59. (Withdrawn) The method of claim 47 wherein the step of forming the high stress LTO layer comprises flowing silane into a reaction chamber with a flow between 50 and 1000 sccm.

60. (Withdrawn) The method of claim 59 wherein the high stress LTO layer is formed at a temperature between 250 and 600°C.

61. (Withdrawn) The method of claim 58 wherein the step of forming the high stress LTO layer further comprises flowing N_2 into the reaction chamber with a flow rate between 800 and 7000 sccm and flowing N_2O into the reaction chamber with a flow rate between 2000 and 18000 sccm.

62. (Withdrawn) The method of claim 47 wherein the steps of forming the low stress and high stress LTO layers include the step of forming a network between the low stress and high stress LTO layers.

63. (Withdrawn) The method of claim 47 wherein the wafer is a p-type silicon wafer or an n-type silicon wafer.

64. (Currently Amended) A ~~backside sealable~~ wafer ~~structure, the wafer structure~~ having a two layer backside seal, comprising:

a wafer substrate having a first major side and second major side and a two layer backside seal comprising;

a low stress LPPECVD-LTO low temperature oxide layer having a first major side and a second major side, the first major side of the low stress LPPECVD-LTO layer being adjacent to the first major side of the wafer substrate; and

a high stress LPPECVD-LTO layer having a first major side and a second major side, the first major side of the high stress LPPECVD-LTO layer being adjacent to the second major side of ~~disposed over~~ the low stress LPPECVD-LTO layer; and

wherein the stress in the low stress LPPECVD-LTO layer is less than 100 MPa and the stress in the high stress LPPECVD-LTO layer is less than 300 MPa and the stress in the high stress LPPECVD-LTO layer is higher than the stress in the low stress LPPECVD-LTO layer.

65. (Currently Amended) The wafer ~~structure of~~ as claimed in claim 64, wherein the wafer substrate comprises ~~further comprising~~ a layer of polysilicon which

is adjacent to the first major side of ~~between the wafer substrate and~~ the low stress LPPECVD-LTO layer.

66. (Currently Amended) The wafer ~~structure of claim 64~~ as claimed in claim 64, wherein the wafer substrate is a p+ substrate ~~or a n+ substrate~~ and wherein an epitaxial layer is adjacent to the second major side of the wafer substrate.

67. (New) The wafer as claimed in claim 64, wherein the wafer substrate is a n+ substrate and wherein an epitaxial layer is adjacent to the second major side of the wafer substrate.